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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,225	03/23/2004	Robert P. Masleid	TRAN-P249	5029

7590 01/24/2007

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EXAMINER	
MAI, ANH D	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,225	MASLEID ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-62* is/are pending in the application.

4a) Of the above claim(s) *32-38 and 47-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 16, 2006 has been entered.

Status of the Claims

2. Amendment filed November 16, 2006 is acknowledged. Claims 32-62 are pending. Non-elected, claims 32-38 and 47-62 have been withdrawn. Action on merits of claims 39-46 follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 39-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr (U.S. Patent No. 6,218,708) of record.

With respect to claim 39, Burr teaches an integrated circuit as claimed including:

a plurality of transistors (302, 304) having a principal operating voltage;

a deep n well capacitor structure comprising:

a deep n well (309) comprising n-material coupled to the principal operating voltage; and

p-type material (p) disposed proximate the deep n well and coupled to the ground reference. (See Fig. 3-6).

Regarding the operating voltage and ground reference, the Vnw (nwell voltage) is the same as Vdd, since the Vnw is split from Vdd and is coupled to the n well, thus called nwell voltage (Vnw). Similarly, Vpw is split from gnd and is coupled to p material, thus called Vpw. (See Figs 1 and 2).

Regarding the term capacitor structure, since the structure of Burr comprises all elements of the claimed structure, thus the n well structure of Burr is capable of functioning as a capacitor. Furthermore, Burr explicitly teaches that "the wells function to hold a substrate potential and are characterized by a high capacitance", hence capacitor structure. (See col. 4, lines 14-16).

With respect to claim 40, wherein the deep n well (309) of Burr is substantially surrounded by p type material (p).

With respect to claim 41, the integrated circuit of Burr comprises a plurality of deep n wells (503). (See Fig. 5).

With respect to claim 42, the deep n well (309) of Burr is parasitically coupled to the principal operating voltage (Vnw).

With respect to claim 43, the p type material (p) of Burr comprises epitaxy.

With respect to claim 44, the p type material (p) of Burr comprises bulk p material.

With respect to claim 45, the p type material (p) of Burr comprises a p well.

With respect to claim 46, the p well (p) of Burr is at substantially a same depth as said deep n well (503). (See Fig. 5).

Response to Arguments

4. Applicant's arguments filed November 16, 2006 have been fully considered but they are not persuasive.

Applicant argues:

> With regard to Claim 1, the Office refers to Burr to support the assertion that Burr teaches "the Vnw (nwell voltage) is the same, since Vnw is split from Vdd and is coupled to the n well, thus called nwell voltage (Vnw)" and "Vpw is split from gnd and is coupled to p material, thus called Vpw (See Figs 1 and 2). The applicants respectfully disagree with the Office's position, and suggest that Burr does not support the Office's assertion.

From Fig. 1a, PMOS 102, V_{dd} contact both source 108 and back bias contact 113, which means the bias to the device and the n-well is the same, or another word, the same principle operating voltage V_{dd} is coupled to the transistor 102 and the n-well 211. Therefore, Burr '708 clearly support the Office's assertion.

Burr '708 recognizes the inefficiency of the design of Figs. 1 and 2, since all of the bias voltages are provided from the surface of the transistors. When the devices are multiplied and the sizes are reduced, this form of wiring would present a challenge. (See col. 2, ll. 46-67).

Burr '708 teaches: "It is a further object of the present invention is to provide a back biased MOS device structure an method which facilitate retrofitting of standard MOS design into back biased configurations without substantially impacting the standard design layout". (See Col. 3, lines 4-9).

The above means the fundamental operations and designs of the standard MOS are unchanged, the only change is the location of back bias, which is provided by the deep N-well 309.

For that reason, claim 39 and the dependent claims 40-46 are clearly anticipated by Burr '708, the rejection thus maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER